CLAIMS

Claims 1-6 were previously cancelled without prejudice.

7. (Previously Presented) A circuit for storing data, said circuit comprising:

a FIFO for queuing the data;

a read pointer for indicating a particular address in the FIFO;

a write pointer for indicating another particular address in the FIFO;

a first Gray code to binary converter for generating the particular address indicated by the read pointer;

a second Gray code to binary converter for generating the another particular address indicated by the write pointer; and

a comparator for determining whether the FIFO is empty or full based on a comparison of a Gray code associated with the read pointer and a Gray code associated with the write pointer.

8. (Previously Presented) The circuit of claim 7, further comprising:

a first Gray code generator for generating the Gray code associated with the read pointer; and

a second Gray code generator for generating the Gray code associated with the write pointer.

9. (Previously Presented) The circuit of claim 8,

wherein the first Gray code to binary converter receives the Gray code associated with the read pointer from the first Gray code generator; and

wherein the second Gray code to binary converter receives the Gray code associated with the write pointer from the second Gray code generator.

10. (Previously Presented) The circuit of claim 7, wherein the FIFO comprises a FIFO RAM.

11. (Previously Presented) A method for storing data, said method comprising:

queuing the data in a FIFO;

indicating a particular read address in the FIFO;

indicating a particular write address in the FIFO;

generating the particular read address by converting a first Gray code to binary;

generating the particular write address by converting a second Gray code to binary; and

determining whether the FIFO is empty or full based on a comparison of the first Gray code associated and the second Gray code.